WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a recess therein;

a gate insulator on the substrate in the recess;

a gate electrode comprising a first portion on the gate insulator in the recess and a second reduced-width portion extending from the first portion; and

a source/drain region in the substrate adjacent the recess.

2. The semiconductor device of claim 1, wherein the gate insulator comprises:

a first portion disposed on a sidewall of the recess and having a first thickness; and

a second portion disposed on a bottom of the recess and having a second thickness less than the first thickness.

3. The semiconductor device of claim 2, wherein the first portion of the gate insulator adjoins a source/drain region in the substrate.

4. The semiconductor device of claim 2, further comprising a nitride liner disposed between the first portion of the gate insulator and the recessed portion of the gate electrode.

5. The semiconductor device of Claim 2, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode and on the insulation layer.

6. The semiconductor device of Claim 5, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

7. The semiconductor device of Claim 5, wherein the insulating spacer comprises a first insulating spacer and further comprising a second insulating spacer on sidewalls of the insulation layer and the first insulating spacer.

8. The semiconductor device of Claim 7, wherein the source/drain region comprises a lighter-doped portion adjoining the recess.

9. The semiconductor device of Claim 1, wherein the gate electrode further comprises a third portion on the second portion, the third portion having ~~a~~ an greater width than the second portion.

10. The semiconductor device of Claim 9, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode, on a sidewall of the third portion of the gate electrode and on the insulation layer.

11. The semiconductor device of Claim 10, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

12. The semiconductor device of Claim 9, wherein the gate insulator comprises:

a first portion disposed on a sidewall of the recess and having a first thickness; and

a second portion disposed on a bottom of the recess and having a second thickness less than the first thickness.

13. The semiconductor device of Claim 12, wherein the source/drain region comprises a lighter-doped portion adjoining the first portion of the gate insulator.

14. The semiconductor device of Claim 9, wherein the gate insulator comprises a substantially uniform thickness insulation layer lining the recess.

15. The semiconductor device of Claim 1, wherein the source/drain region comprises a lighter-doped portion nearer the recess.

16. The semiconductor device of Claim 1, wherein the recess has a curved shape.

17. The semiconductor device of Claim 16, wherein the recess is hemispherical or elliptical.

18. A method of forming a semiconductor device, comprising:

forming an insulation layer on a substrate;

forming a sacrificial layer on the insulation layer;

forming an opening through the sacrificial layer and the insulation layer to expose an active region of the substrate;

removing a portion of the active region to form a recess therein that has a greater width than the opening through the sacrificial layer and the insulation layer;

forming a gate insulator in the recess;

forming a gate electrode extending through the sacrificial layer and the insulation layer and into the recess, the gate electrode comprising a first portion on the gate insulator in the recess and a second reduced-width portion extending from the first portion;

removing the sacrificial layer to expose a sidewall of the gate electrode outside of the recess;

forming an insulating spacer on the exposed sidewall of the gate electrode; and

forming a source/drain region in the substrate adjacent the recess.

19. The method as claimed in claim 18, wherein the forming a gate insulator comprises:

forming a first insulating layer having a first thickness in the recess;

removing a portion of the first insulating layer on a bottom of the recess to expose a bottom of the recess while leaving a portion of the first insulating layer on a sidewall of the recess; and

forming a second insulation layer on the exposed bottom of the recess, the second insulation layer having a second thickness less than the first thickness.

20. The method of Claim 19, wherein removing a portion of the first insulating layer is preceded by forming a nitride liner on the first insulation layer, wherein removing a portion of the first insulating layer on a bottom of the recess to expose a bottom of the recess while leaving a portion of the first insulating layer on a sidewall of the recess comprises removing portions of the first insulating layer and the nitride liner on the bottom of the recess to expose the bottom of the recess while leaving portions of the first insulating layer and the nitride liner on a sidewall of the recess.

21. The method of Claim 18, wherein removing a portion of the active region to form a recess therein is preceded by forming a sidewall spacer on a sidewall of the sacrificial layer and the insulation layer, and wherein removing a portion of the exposed active region comprises etching the exposed active region using the sidewall spacer as an etching mask.

22. The method of Claim 21, wherein forming a gate electrode comprises depositing a conductive material through an opening defined by the sidewall spacer.

23. The method of Claim 18, wherein forming an opening comprises:

removing a portion of the sacrificial layer overlying the active region to expose the insulation layer;

forming a sidewall spacer on a sidewall of the sacrificial layer; and

etching an exposed portion of the insulation layer using the sidewall spacer as an etching mask to expose a portion of the active region.

24. The method of Claim 18, wherein forming an opening comprises:

removing a portion of the sacrificial layer overlying the active region without exposing the insulation layer;

forming a sidewall spacer on a sidewall of the sacrificial layer; and

etching through portions of the sacrificial layer and the insulation layer using the sidewall spacer as an etching mask to expose a portion of the active region.

25. The method of Claim 24, wherein forming a gate electrode comprises:

removing the sidewall spacer to form an enlarged opening through at least one portion of the sacrificial layer; and

depositing conductive material into the enlarged opening.

26. The method of Claim 18:

wherein forming an insulating spacer comprises forming a first insulating spacer on the exposed sidewall of the gate electrode;

wherein forming a source/drain region comprises implanting ions into the substrate using the first insulating spacer as an implantation mask;

wherein forming an insulating spacer further comprises forming a second insulating spacer on the first insulating spacer; and

wherein forming a source/drain region comprises implanting ions into the substrate using the second insulating spacer as an implantation mask to thereby form a source/drain region comprising lighter and heavier doped portions.

27. The method of Claim 18, further comprising forming a planarization buffer layer on the sacrificial layer, wherein forming an opening through the sacrificial layer and the insulation layer to expose an active region of the substrate comprises forming an opening through the planarization buffer layer, the sacrificial layer and the insulation layer, and wherein forming a gate electrode extending through the sacrificial layer and the insulation layer and into the recess comprises:

depositing a conductive material in the opening through the planarization buffer layer, the sacrificial layer and the insulation layer; and

planarizing the substrate to remove the planarization buffer layer and a portion of the deposited conductive material overlying the sacrificial layer.

28. A semiconductor device comprising:

a semiconductor substrate having a recess;

a gate electrode comprising a recessed gate electrode portion filling the recess

and a protruding gate electrode portion connected to the recessed gate electrode portion and protruding from the semiconductor substrate; and

an insulator interposed between the semiconductor substrate and the recessed gate electrode portion,

wherein the protruding gate electrode portion comprises a bottom gate electrode portion connecting to the recessed gate electrode portion and having a narrower width than that of the recess and a main gate electrode portion connecting to the bottom gate electrode portion and having a wider width than that of the recess.

29. The semiconductor device as claimed in claim 28, wherein the insulator comprises:

a buffer gate insulator having a first thickness on both sidewalls of the recess; and

a gate insulator having a second thickness thinner than the first thickness and connecting to the buffer gate insulator on a bottom of the recess.

30. The semiconductor device as claimed in claim 29, wherein ends of the gate insulator are aligned with outer sidewalls of the bottom gate electrode portion.

31. The semiconductor device as claimed in claim 30, wherein the main gate electrode portion comprises a main gate electrode center portion having the same gate length with the bottom gate electrode portion and connecting to the bottom gate electrode portion; and a silicide spacer disposed on both sidewalls of the main gate electrode center portion, and an end point of the recess is located between an outer sidewall of the silicide spacer and an outer sidewall of the bottom gate electrode portion.

32. The semiconductor device as claimed in claim 29, further comprising a nitride liner disposed on a part of the buffer gate insulator and on both sidewalls of the protruding gate electrode portion.

33. The semiconductor device as claimed in claim 31, further comprising:

a buffer insulator formed on both sidewalls of the bottom gate electrode portion and aligned with outer sidewalls of the metal silicide spacer;

an insulation spacer disposed on outer sidewalls of the buffer insulator and the metal silicide spacer; and

a metal silicide layer disposed on an upper surface of the main gate electrode center portion and on the semiconductor substrate adjacent to both sidewalls of the insulation spacer.

34. The semiconductor device as claimed in claim 28, further comprising:

an insulation spacer disposed on outer sidewalls and bottom surfaces of the main gate electrode portion; and

a buffer insulator disposed on outer sidewalls of the bottom gate electrode portion and aligned with outer sidewalls of the insulation spacer.

35. The semiconductor device as claimed in claim 33, wherein the buffer insulator is formed of oxide and the insulation spacer is formed of nitride.

36. The semiconductor device as claimed in claim 34, wherein the buffer insulator is formed of oxide and the insulation spacer is formed of nitride.

37. The semiconductor device as claimed in claim 28, wherein the recess has a smooth curved surface.

38. The semiconductor device as claimed in claim 33, further comprising:

a low concentration impurity-doped region in the semiconductor substrate under the buffer insulator and the insulation spacer; and

a high concentration impurity-doped region connecting to the low concentration impurity-doped region in the semiconductor substrate adjacent to the insulation spacer.

39. The semiconductor device as claimed in claim 34, further comprising:

a low concentration impurity-doped region in the semiconductor substrate under the buffer insulator and the insulation spacer; and

a high concentration impurity-doped region connecting to the low concentration impurity-doped region in the semiconductor substrate adjacent to the insulation spacer.